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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/818,115	03/27/2001	Steven J. Tinsley	TI-31546	1919

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EXAMINER	
MANOSKEY, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2184	3

DATE MAILED: 12/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/818,115	TINSLEY ET AL.	
	Examiner	Art Unit	
	Joseph Manoskey	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 8 is objected to because of the following informalities: the word "or" should be removed from line 13. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 8-11, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (hereinafter referred to as APA) in view of Erckert, U.S. Patent 6,493,401.

4. Referring to claim 1, the APA teaches a failsafe detection apparatus for a differential receiver comprising a window comparator, a timer for the bus activity signal, and a failsafe indicator gate coupled with the timer and window comparator (See Fig. 2). The APA does not teach the timer being coupled to both the bus activity signal and the output of the window comparator, however the APA does disclose that the activity timer's purpose is to provide a time for how long invalid data may exist on the bus before a failsafe signal is issued (See page 9, lines 4-6). Erckert discloses a receiving circuit that contains a window comparator that is connected to a timer (See Fig. 1). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the timer and window comparator of Erckert with the timer the APA to have a

timer that receives inputs from both the bus activity signal and the output of the window comparator. This would be obvious to one of ordinary skill in the art at the time of the invention was made to do because the timer of Erckert insures that no logic values changed on the window comparator for more than a predetermined amount of time resulting in a violation of protocol or error in data (See Col. 3, lines 7-13).

5. Referring to claim 2, the APA and Erckert disclose all the limitations (See rejection of claim 1) including the failsafe indicator gate comprising an OR gate (See Fig. 2).

6. Referring to claim 3, the APA and Erckert teach all the limitations (See rejection of claim 1) including the window comparator comprising first and second comparators configured to compare differential data with respective first and second references that represent a failsafe threshold and a logic gate coupled to the outputs of the comparators (See Fig. 2 of the APA).

7. Referring to claim 4, the APA and Erckert disclose all the limitations (See rejection of claim 3), however they are silent on the use of an XOR gate being used to couple the bus activity gate and the window comparator output to the timer. It would be obvious to one of ordinary skill in the art at the time of the invention to use an XOR gate to couple the bus activity gate and window comparator to the timer. This would be obvious to one of ordinary skill in the art when the invention was made because the failsafe circuit would not function properly otherwise.

8. Referring to claim 8, the APA teaches a system for failsafe detection of a differential receiver comprising a differential input device, a fault detection device, a

resettable timer for the bus activity signal, and a failsafe indicator gate coupled with the timer and window comparator (See Fig. 1 and 2). The APA does not teach the timer being coupled to both the bus activity signal and the output of the window comparator, however the APA does disclose that the activity timer's purpose is to provide a time for how long invalid data may exist on the bus before a failsafe signal is issued (See page 9, lines 4-6). Erckert discloses a receiving circuit that contains a window comparator that is connected to a timer (See Fig. 1). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the timer and window comparator of Erckert with the timer the APA to have a timer that receives inputs from both the bus activity signal and the output of the window comparator. This would be obvious to one of ordinary skill in the art at the time of the invention was made to do because the timer of Erckert insures that no logic values changed on the window comparator for more than a predetermined amount of time resulting in a violation of protocol or error in data (See Col. 3, lines 7-13).

9. Referring to claim 9, the APA and Erckert disclose all the limitations (See rejection of claim 8) including the failsafe indicator gate comprising an OR gate (See Fig. 2 of the APA).

10. Referring to claim 10, the APA and Erckert teach all the limitations (See rejection of claim 8) including the window comparator comprising first and second comparators configured to compare differential data with respective first and second references that represent a failsafe threshold and a logic gate coupled to the outputs of the comparators (See Fig. 2 of the APA).

11. Referring to claim 11, the APA and Erckert disclose all the limitations (See rejection of claim 10), however they are silent on the use of an XOR gate being used to couple the bus activity gate and the window comparator output to the timer. It would be obvious to one of ordinary skill in the art at the time of the invention to use an XOR gate to couple the bus activity gate and window comparator to the timer. This would be obvious to one of ordinary skill in the art when the invention was made because the failsafe circuit would not function properly otherwise.

12. Referring to claim 15, the APA teaches a method of providing failsafe detection in differential receiver circuit comprising detecting a receive threshold transition and commencing a count down and detecting a failsafe threshold transition (See Fig. 1 and 2). The APA does not teach a count down being commenced when a failsafe threshold transition occurs, however the APA does disclose that the activity timer's purpose is to provide a time for how long invalid data may exist on the bus before a failsafe signal is issued (See page 9, lines 4-6). Erckert discloses a receiving circuit that contains a window comparator that is connected to a timer (See Fig. 1). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the timer and window comparator of Erckert with the timer the APA to have a timer that receives inputs from both the bus activity signal and the output of the window comparator so that a countdown will commence when both a receive threshold transition and failsafe threshold transition are detected. This would be obvious to one of ordinary skill in the art at the time of the invention was made to do because the timer of Erckert insures that no logic values changed on the window comparator for more than a predetermined

amount of time resulting in a violation of protocol or error in data (See Col. 3, lines 7-13).

13. Referring to claim 16, the APA and Erckert disclose all the limitations (See rejection of claim 15) including the failsafe indicator gate comprising an OR gate (See Fig. 2 of the APA).

14. Referring to claim 17, the APA and Erckert teach all the limitations (See rejection of claim 15) including using first logic gate to receive both indications of threshold transitions (See Fig. 2 of the APA) however they are silent on the use of a second logic gate being used to couple the bus activity gate and the window comparator output to the timer. It would be obvious to one of ordinary skill in the art at the time of the invention to use a second logic gate to couple the bus activity gate and window comparator to the timer. This would be obvious to one of ordinary skill in the art when the invention was made because the failsafe circuit would not function properly otherwise

15. Referring to claim 18, the APA and Erckert disclose all the limitations (See rejection of claim 15), however they are silent on the use of an XOR gate being used to couple the bus activity gate and the window comparator output to the timer. It would be obvious to one of ordinary skill in the art at the time of the invention to use an XOR gate to couple the bus activity gate and window comparator to the timer. This would be obvious to one of ordinary skill in the art when the invention was made because the failsafe circuit would not function properly otherwise.

16. Claims 5-7, 12-14, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the APA and Erckert in view of Shirai et al., U.S. Patent 5,867,775.

17. Referring to claim 5, the APA and Erckert teach all the limitations (See rejection of claim 1) except for a delay circuit coupled between the window comparator and the failsafe indicator circuit, however Erckert does teach the use of a switch that changes after the timer expires thus delaying the output (See Col. 3, lines 13-17). Shirai et al. teaches the use of a failsafe delay circuit coupled to the output of a failsafe window comparator (See Fig. 3). It would be obvious to one of ordinary skill in the art at the time of the invention to connect the delay circuit of Shirai et al. to the output of the window comparator of the APA and Erckert. This would have been obvious to one of ordinary skill in the art when the invention was made to do because it provides a delay needed for waiting until the timer expires in order for the circuit to function properly.

18. Referring to claim 6, the APA, Erckert, and Shirai et al. teach all the limitations (See rejection of claim 5). Although Shirai et al. is silent on the length of the delay time of the delay circuit, it would inherently be longer then the time it takes for the timer to expire. If the delay time did not exceed the expiration time of the failsafe circuit would not function properly.

19. Referring to claim 7, the APA, Erckert, and Shirai et al. teach all the limitations (See rejection of claim 6) including the delay circuit being a RC circuit. Shirai teaches the delay circuit being a "CR circuit" (See Col. 7, lines 61-62), which is interpreted as a RC circuit.

20. Referring to claim 12, the APA and Erckert teach all the limitations (See rejection of claim 8) except for a delay circuit coupled between the window comparator and the failsafe indicator circuit, however Erckert does teach the use of a switch that changes

after the timer expires thus delaying the output (See Col. 3, lines 13-17). Shirai et al. teaches the use of a failsafe delay circuit coupled to the output of a failsafe window comparator (See Fig. 3). It would be obvious to one of ordinary skill in the art at the time of the invention to connect the delay circuit of Shirai et al. to the output of the window comparator of the APA and Erckert. This would have been obvious to one of ordinary skill in the art when the invention was made to do because it provides a delay needed for waiting until the timer expires in order for the circuit to function properly.

21. Referring to claim 13, the APA, Erckert, and Shirai et al. teach all the limitations (See rejection of claim 6). Although Shirai et al. is silent on the length of the delay time of the delay circuit, it would inherently be longer then the time it takes for the timer to expire. If the delay time did not exceed the expiration time of the failsafe circuit would not function properly.

22. Referring to claim 14, the APA, Erckert, and Shirai et al. teach all the limitations (See rejection of claim 13) including the delay circuit being a RC circuit. Shirai teaches the delay circuit being a "CR circuit" (See Col. 7, lines 61-62), which is interpreted as a RC circuit.

23. Referring to claim 19, the APA and Erckert teach all the limitations (See rejection of claim 15) except for a delay circuit coupled between the window comparator and the failsafe indicator circuit (the second detecting step), however Erckert does teach the use of a switch that changes after the timer expires thus delaying the output (See Col. 3, lines 13-17). Shirai et al. teaches the use of a failsafe delay circuit coupled to the output of a failsafe window comparator (See Fig. 3). It would be obvious to one of ordinary skill

in the art at the time of the invention to connect the delay circuit of Shirai et al. to the output of the window comparator of the APA and Erckert. This would have been obvious to one of ordinary skill in the art when the invention was made to do because it provides a delay needed for waiting until the timer expires in order for the circuit to function properly.

24. Referring to claim 20, the APA, Erckert, and Shirai et al. teach all the limitations (See rejection of claim 19). Although Shirai et al. is silent on the length of the delay time of the delay circuit, it would inherently be longer then the time it takes for the timer to expire. If the delay time did not exceed the expiration time of the failsafe circuit would not function properly.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,147,515 to Ang et al.

U.S. Patent 6,111,437 to Patel et al.

U.S. Patent 5,488,306 to Bonaccio

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone

number for the organization where this application or proceeding is assigned is (703)-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JDM
November 26, 2003

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
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